REMARKS

Claim 10 is amended to correct a typographical error.

Claims 1 – 58 are rejected pursuant to 35 U.S.C. §102(e) as being anticipated by Nakamura (U.S. Pat. Pub. No.: 2002/0078316). With respect to claim 1, the Examiner stated:

> Nakamura teaches the invention (claim 1) as claimed including a combination comprising: a processor as the processing circuit (e.g., see Figure 1, element 2); and a transparent memory array comprising a plurality of memory banks, each of the plurality of memory banks being directly connected to the processor, the memory array operable to function without at least one of a precharge signal, a row address latch signal and a column address latch signal with the embedded SDRAM teaches a transparent memory array (e.g., see paragraph 0010).

It is respectfully submitted that the Examiner has misconstrued the teachings of Nakamura. More specifically, Nakamura is directed to a SDRAM 4 that consumes less power during a data hold mode. (See paragraph 0059.) The SDRAM 4 disclosed by Nakamura has a clock input buffer 10 that receives an external clock signal (CLK) from a memory controller 3. (See Figures 1 and 2; paragraph 0054.) The clock input buffer 10 uses the external clock signal (CLK) to generate two internal clock signals (CLK1 and CLK2) that are used by the SDRAM 4. (See Figure 2; paragraph 0059.) The first internal clock signal (CLK1) is used to control command input buffer 12, whereas the second internal clock signal (CLK2) is used to control address input buffer 14 and data input buffer 16. (See Figures 2 and 3, paragraph 0059.) Both internal clock signals (CLK1 and CLK2) are active when the SDRAM is in a normal operating mode. (See paragraph 0059.) When the SDRAM is in a data hold mode, the first internal clock signal (CLK1) is active, whereas the second internal clock signal (CLK2) is inactive. (See paragraph 0059.) Nakamura teaches that setting the second internal clock signal (CLK2) inactive during data hold mode, power consumption by the address input buffer 14 and the data input buffer 16 is eliminated. (See paragraph 0059.)

It is respectfully submitted that the portions of Nakamura (i.e., Figure 1; paragraph 0010) cited by the Examiner fail to teach the subject matter recited by claim 1. More specifically, Nakamura is silent as to the role that precharge, row address latch, and column address latch signals have in the operation of SDRAM 4. Thus, it is believed that Nakamura fails to teach or disclose a "memory array operable to function without at least one of a precharge signal, a row address latch signal, and a column address latch signal." as recited in claim 1. Accordingly, it is believe that claim 1 is in condition for allowance and it is respectfully requested that the rejection of claim 1 pursuant to 35 U.S.C. §102(e) be withdrawn.

Claims 2 – 5 depend from allowable claim 1. It is respectfully submitted that the additional portions of Nakamura (e.g., Figure 2; paragraphs 0053 and 0057 – 0059) cited by the Examiner in support of the rejections of claims 2 – 5 also fail to teach the subject matter recited by claim 1. Thus for the same reasons discussed above in conjunction with claim 1, it is believed that claims 2 – 5 are in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 2 – 5 pursuant to 35 U.S.C. §102(e) be withdrawn.

With respect to claim 6, the Examiner stated:

> Nakamura teaches the invention (claim 6) as claimed including a combination comprising a processor as the processing circuit (e.g., see Figure 1, element 2); and a plurality of transparent memory arrays being directly connected to said processor, and each operable to function without at least one of a precharge signal, a row address latch signal, and a column address latch signal with the embedded SDRAM teaches the transparent memory array (e.g., see paragraph 0010).

Claim 6 recites that each transparent memory array is operable "to function without at least one of a precharge signal, a row address latch signal, and a column address latch signal." Thus for the same reasons discussed above in conjunction with claim 1, it is believed that claim 6 is in condition for allowance. Accordingly, it is respectfully requested that the rejection of claim 6 pursuant to 35 U.S.C. §102(e) be withdrawn.

Claims 7 – 10 depend from allowable claim 6. It is respectfully submitted that the additional portions of Nakamura (e.g., Figure 2; paragraphs 0053 and 0057 – 0059) cited by the Examiner in support of the rejections of claims 7 – 10 also fail to teach the subject matter recited by claim 6. Thus for the same reasons discussed above in conjunction with claim 6, it is believed that claims 7 – 10 are in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 7 – 10 pursuant to 35 U.S.C. §102(e) be withdrawn.

With respect to claim 11, the Examiner stated:

> Nakamura teaches the invention (claim 11) as claimed including a combination comprising an integrated circuit having a processor (e.g., see Figure 1, element 2); and an embedded memory array, the memory array having a plurality of controllers and a plurality of memory banks, each of the memory banks being independently connected to one of the plurality of controllers, each of the controllers being independently connected to the processor (e.g., see paragraph 0010).

It is respectfully submitted that the Examiner has misconstrued the teachings of Nakamura. More specifically, Figure 1 merely illustrates a single memory controller 3 connected to the processing circuit 2. Figure 1 fails to teach or disclose "a plurality of controllers ... each of the plurality of controllers being

independently connected to the processor" as recited by claim 11. Furthermore, paragraph 0010 fails provide this missing teaching.

Thus, for the reasons discussed above, it is believed that claim 11 is in condition for allowance. Accordingly, it is respectfully requested that the rejection of claim 11 pursuant to 35 U.S.C. §102(e) be withdrawn.

Claims 12 – 17 depend from allowable claim 11. It is respectfully submitted that the additional portions of Nakamura (e.g., Figure 2; paragraphs 0053 and 0057 – 0059) cited by the Examiner in support of the rejections of claims 12 – 17 also fail to teach the subject matter recited by claim 11. Thus for the same reasons discussed above in conjunction with claim 11, it is believed that claims 12 – 17 are in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 12 – 17 pursuant to 35 U.S.C. §102(e) be withdrawn.

With respect to claim 18, the Examiner stated:

> Nakamura teaches the invention (claim 18) as claimed comprising an integrated circuit having a processor (e.g., see Figure 1, element 2); and an embedded memory array having a plurality of memory banks, each of the memory banks being independently connected to processor (e.g., see paragraph 0010).

It is respectfully submitted that Nakamura fails to teach the claimed invention. More specifically, Figure 1 illustrates a single processing circuit 2, a single memory controller 3, and a single SDRAM 4. As illustrated in Figure 1, the SDRAM 4 is connected to the memory controller 3, but the SDRAM 4 is not independently connected to the processing circuit 2. Figure 1 fails to teach "an embedded memory array having a plurality of memory banks, each of the memory banks being independently connected to processor" as recited by claim 18. Furthermore, paragraph 0010 fails provide this missing teaching.

Thus, for the reasons discussed above, it is believed that claim 18 is in condition for allowance. Accordingly, it is respectfully requested that the rejection of claim 18 pursuant to 35 U.S.C. §102(e) be withdrawn.

Claims 19 – 24 depend from allowable claim 18. It is respectfully submitted that the additional portions of Nakamura (e.g., Figure 2; paragraphs 0053 and 0057 – 0059) cited by the Examiner in support of the rejections of claims 19 – 24 also fail to teach the subject matter recited by claim 18. Thus for the same reasons discussed above in conjunction with claim 18, it is believed that claims 19 – 24 are in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 19 – 24 pursuant to 35 U.S.C. §102(e) be withdrawn.

With respect to claim 25, the Examiner stated:

> Nakamura teaches the invention (claim 25) as claimed including a combination, comprising a processor as the processing circuit (e.g., see Figure 1, element 2); and a plurality of transparent SDRAM arrays directly connected to the processor as embedded SDRAM (e.g., see paragraph 10).

As discussed above in conjunction with claim 18, Figure 1 of Nakamura teaches that the SDRAM 4 is connected to the memory controller 3, not to the processing circuit 2. Thus, Nakamura fails to teach a plurality of memory arrays directly connected to the processor. Furthermore, paragraph 0010 fails to provide this missing teaching. Thus, for these reasons, it is believed that claim 25 is in condition for allowance. Accordingly, it is respectfully requested that the rejection of claim 25 pursuant to 35 U.S.C. §102(e) be withdrawn.

Claims 26 – 30 depend from allowable claim 25. It is respectfully submitted that the additional portions of Nakamura (e.g., Figure 2; paragraphs 0053 and 0057 – 0059) cited by the Examiner in support of the rejections of claims 26 – 30 also fail to teach the subject matter recited by claim 25. Thus for the same reasons discussed above in conjunction with claim 25, it is believed that claims 26 – 30 are in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 26 – 30 pursuant to 35 U.S.C. §102(e) be withdrawn.

With respect to claim 31, the Examiner stated:

> Nakamura teaches the invention (claim 31) as claimed including a combination, comprising a processor as the processing circuit (e.g., see Figure 1, element 2); and a transparent SDRAM having a plurality of memory banks, each of the plurality of memory banks being directly connected to the processor as embedded SDRAM (e.g., see paragraph 10).

As discussed above in conjunction with claim 25, Figure 1 of Nakamura fails to teach a plurality of memory banks directly connected to the processor. Furthermore, paragraph 0010 fails provide this missing teaching. Thus, for these reasons, it is believed that claim 31 is in condition for allowance. Accordingly, it is respectfully requested that the rejection of claim 31 pursuant to 35 U.S.C. §102(e) be withdrawn.

Claims 32 – 36 depend from allowable claim 31. It is respectfully submitted that the additional portions of Nakamura (e.g., Figure 2; paragraphs 0053 and 0057 – 0059) cited by the Examiner in support of the rejections of claims 36 – 36 also fail to teach the subject matter recited by claim 31. Thus for the same reasons discussed above in conjunction with claim 31, it is believed that claims 36 – 36 are in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 32 – 36 pursuant to 35 U.S.C. §102(e) be withdrawn.

With respect to claim 37, the Examiner stated:

> Nakamura teaches the invention (claim 37) as claimed including a combination, comprising a processor as the processing circuit (e.g., see Figure 1, element 2); and a transparent SDRAM having a plurality of memory banks connected to the processor such that the processor may simultaneously access more than one of the plurality of memory banks as embedded SDRAM (e.g., see paragraph 10).

As discussed above, Nakamura is directed to a SDRAM 4 that is capable of reducing the amount of power consumed during a data hold mode. (See paragraph 0059.) Figure 1 illustrates a single processing circuit 2, a single memory controller 3, and a single SDRAM 4 (which may have a plurality of memory banks as illustrated in Figure 2). Figure 1, however, fails to teach or disclose that the processing circuit 2 "may simultaneously access more than one of the plurality of memory banks."

More specifically as illustrated in Figure 1, the processing circuit 2 communicates with the memory controller 3 via a command bus (CMDBus) and an address bus (ADBus). The memory controller 3, in turn, sends the external clock signal (CLK), a clock enable signal (CKE), a command signal (CMD), address signals ($A_0 \sim A_n$) and data signals ($DI_0 \sim DI_n$) to the SDRAM 4 and receives data signals ($DO_0 \sim DO_n$) from the SDRAM 4. However, not only does Figure 1 of Nakamura fail to teach or disclose that the signals between the processing circuit 2 and the memory controller 3 are operable to simultaneously access a plurality of memory banks, but Figure 1 also fails to teach or disclose that the signals between the memory controller 3 and the SDRAM 4 are operable to simultaneously access a plurality of memory banks. Furthermore, paragraph 0010 fails to provide this missing teaching.

Thus, for these reasons, it is believed that claim 37 is in condition for allowance. Accordingly, it is respectfully requested that the rejection of claim 37 pursuant to 35 U.S.C. §102(e) be withdrawn.

Claims 38 – 42 depend from allowable claim 37. It is respectfully submitted that the additional portions of Nakamura (e.g., Figure 2; paragraphs 0053 and 0057 – 0059) cited by the Examiner in support of the rejections of claims 38 – 42 also fail to teach the subject matter recited by claim 37. Thus for the same reasons discussed above in conjunction with claim 37, it is believed that claims 38 – 42 are in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 38 – 42 pursuant to 35 U.S.C. §102(e) be withdrawn.

With respect to claim 43, the Examiner stated:

> Nakamura teaches the invention (claim 43) as claimed including a transparent memory array comprising a plurality of memory banks each comprised of a plurality of memory cells (e.g., see Figure 2) and a plurality of peripheral devices including a plurality of controllers, one or each of the plurality of controllers connected to one each of the plurality of memory banks and wherein the plurality of controllers is operable to

simultaneously communicate with a processor (e.g., see Figure 2 and paragraphs 0056 – 0060).

As discussed above in conjunction with claim 37, Nakamura fails to teach or disclose that a plurality of controllers connected to one each of the plurality of memory banks is operable to simultaneously communicate with a processor.

Thus, for the same reasons discussed above in conjunction with claim 37, it is believed that claim 43 is in condition for allowance. Accordingly, it is respectfully requested that the rejection of claim 43 pursuant to 35 U.S.C. §102(e) be withdrawn.

Claims 44 – 48 depend from allowable claim 43. Thus for the same reasons discussed above in conjunction with claim 43, it is believed that claims 44 – 48 are in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 44 – 48 pursuant to 35 U.S.C. §102(e) be withdrawn.

With respect to claim 49, the Examiner stated:

Nakamura teaches the invention (claim 49) as claimed including a method for decreasing the access latency of an integrated circuit having a processor and a plurality of embedded memory arrays having a plurality of memory banks, the method comprising: connecting each of the plurality of memory banks to the processor (e.g., see Figure 2 and paragraphs 0056 – 0060) and simultaneously accessing at least two of the plurality of embedded memory banks with the processor (e.g., see Figure 2 and paragraphs 0056 – 0060).

As discussed above in conjunction with claims 37 and 43, Nakamura fails to teach or disclose that a plurality of controllers connected to one each of the plurality of memory banks is operable to simultaneously communicate with a processor. Furthermore, Nakamura fails to teach or disclose a method comprising "simultaneously accessing at least two of the plurality of embedded memory banks with the processor."

Thus, for the same reasons discussed above in conjunction with claims 37 and 43, it is believed that claim 49 is in condition for allowance. Accordingly, it is respectfully requested that the rejection of claim 49 pursuant to 35 U.S.C. §102(e) be withdrawn.

Claims 50 – 51 depend from allowable claim 49. Thus for the same reasons discussed above in conjunction with claim 49, it is believed that claims 50 – 51 are in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 50 – 51 pursuant to 35 U.S.C. §102(e) be withdrawn.

With respect to claim 52, the Examiner stated:

> Nakamura teaches the invention (claim 52) as claimed including a method for increasing the throughput of an integrated circuit having a processor and an transparent SDRAM array, the transparent SDRAM array having a controller, a data bus, and a plurality of memory banks, each of the plurality of memory banks being independently connected to the controller, the method comprising at least one of simultaneously reading data from more than one of the plurality of memory banks (e.g., see Figure 2 and paragraphs 0056 – 0060); and simultaneously writing data from more than one of the plurality of memory banks (e.g., see Figure 2 and paragraphs 0056 – 0060).

As discussed above in conjunction with claims 37, 43, and 49, Nakamura fails to teach or disclose that a plurality of controllers connected to one each of the plurality of memory banks is operable to simultaneously communicate with a processor and/or a method comprising "simultaneously accessing at least two of the plurality of embedded memory banks with the processor." Thus, Nakamura fails to teach or disclose a method comprising "at least one of simultaneously reading data from more than one of the plurality of memory banks and simultaneously writing data from more than one of the plurality of memory banks."

Thus, for the same reasons discussed above in conjunction with claims 37, 43, and 49, it is believed that claim 52 is in condition for allowance. Accordingly, it is respectfully requested that the rejection of claim 49 pursuant to 35 U.S.C. §102(e) be withdrawn.

Claims 53 – 58 depend from allowable claim 52. Thus for the same reasons discussed above in conjunction with claim 52, it is believed that claims 53 – 58 are in condition for allowance. Accordingly, it is respectfully requested that the rejection of claims 53 – 58 pursuant to 35 U.S.C. §102(e) be withdrawn.

Applicants have made a diligent effort to place the claims in condition for allowance. Accordingly, a Notice of Allowance for claims 1 – 58 is respectfully requested. If the Examiner is of the opinion that the instant application is in condition for disposition other than through allowance, the Examiner is respectfully requested to contact applicants' attorney at the telephone number listed below so that additional changes may be discussed.

Respectfully submitted,

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Amendments to the Drawing figures:

Six (6) sheets of replacement drawings are submitted herewith. The replacement sheets include labels for the elements in FIG. 1 through FIG. 6 as required by the Examiner. No new matter is added. It should be noted that FIG. 7 remains unchanged. Thus, a replacement sheet for FIG. 7 has not been submitted.